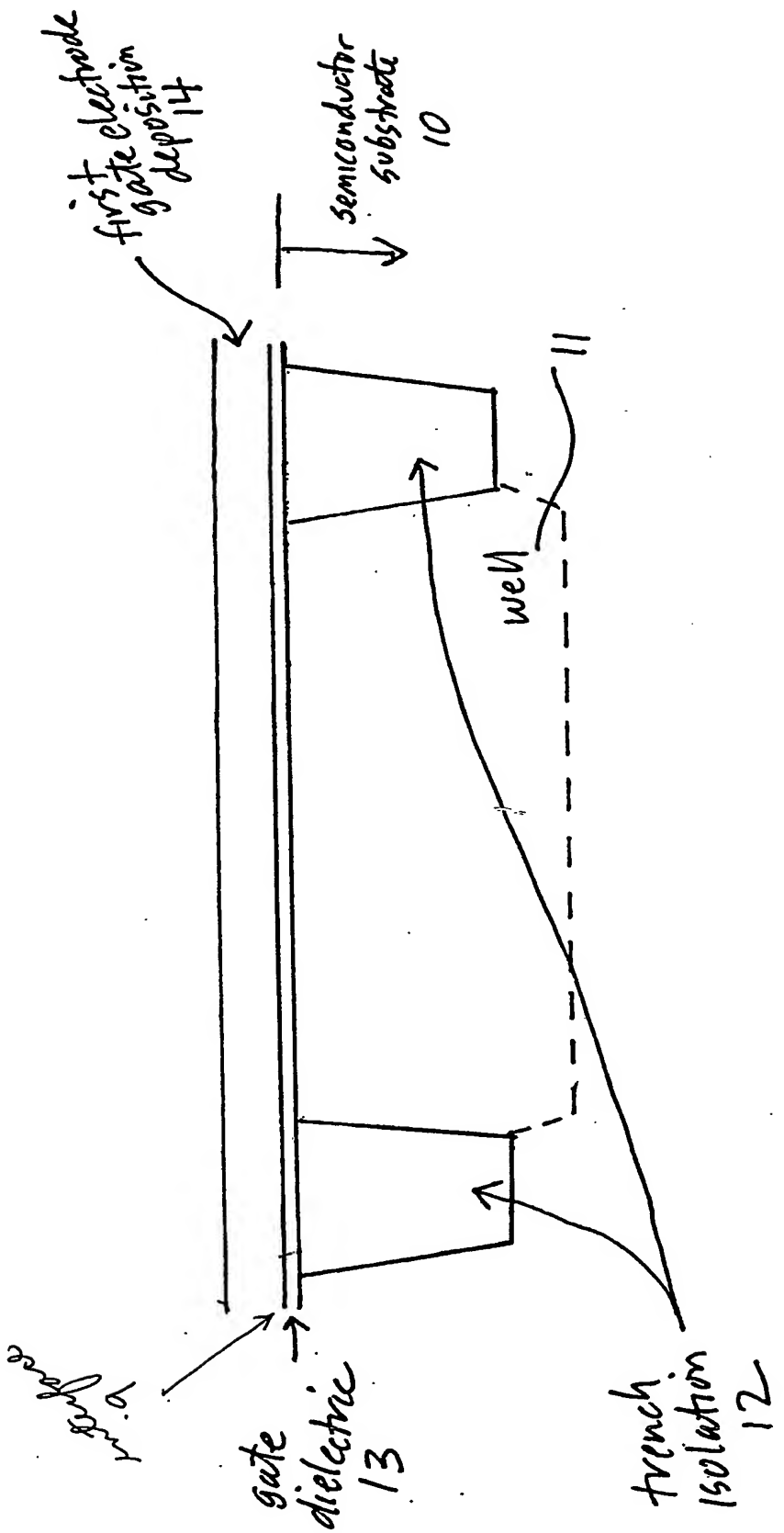

Fig 1a Deposition of first electrode layer

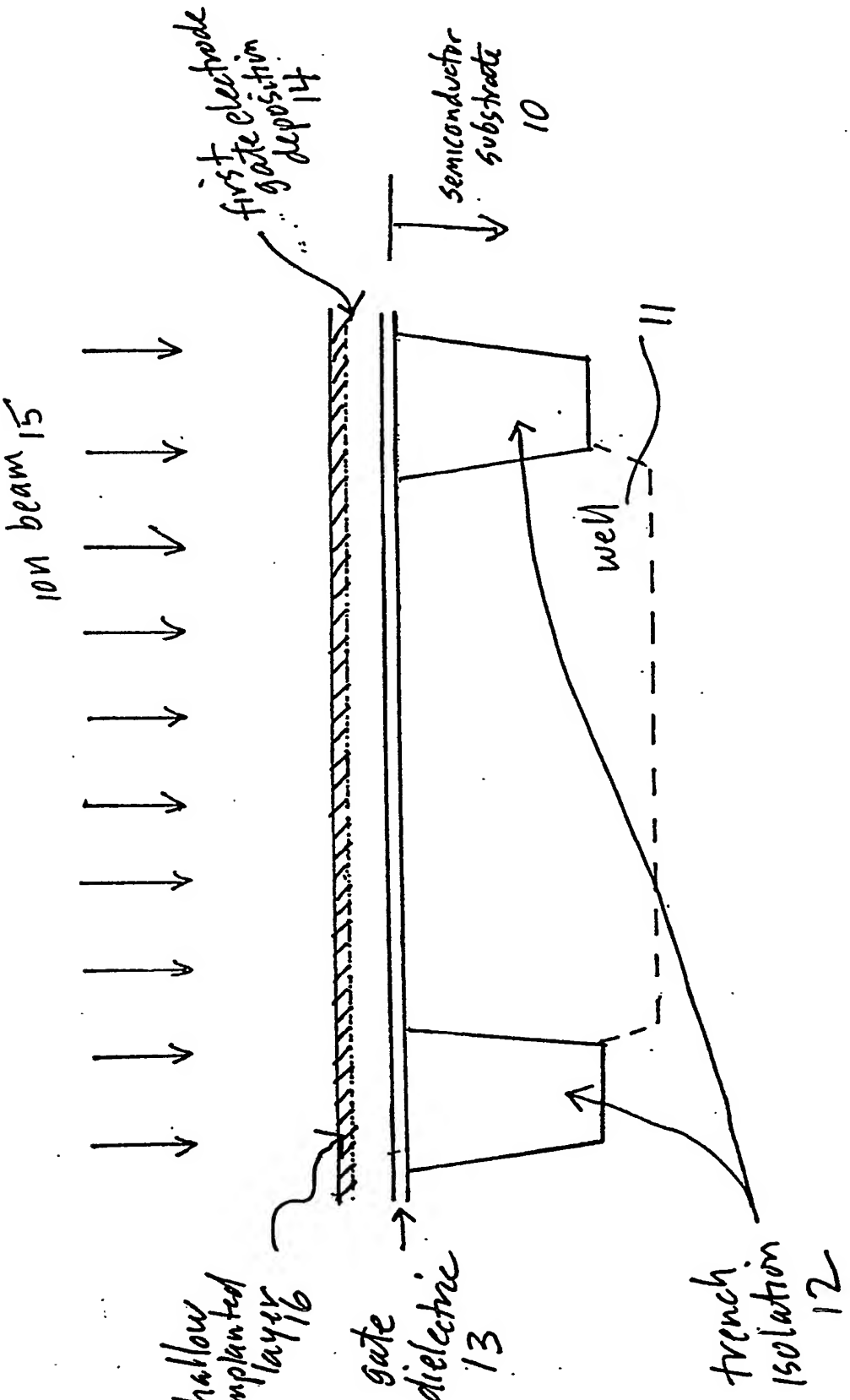

FIG 1B Process through first ion implant

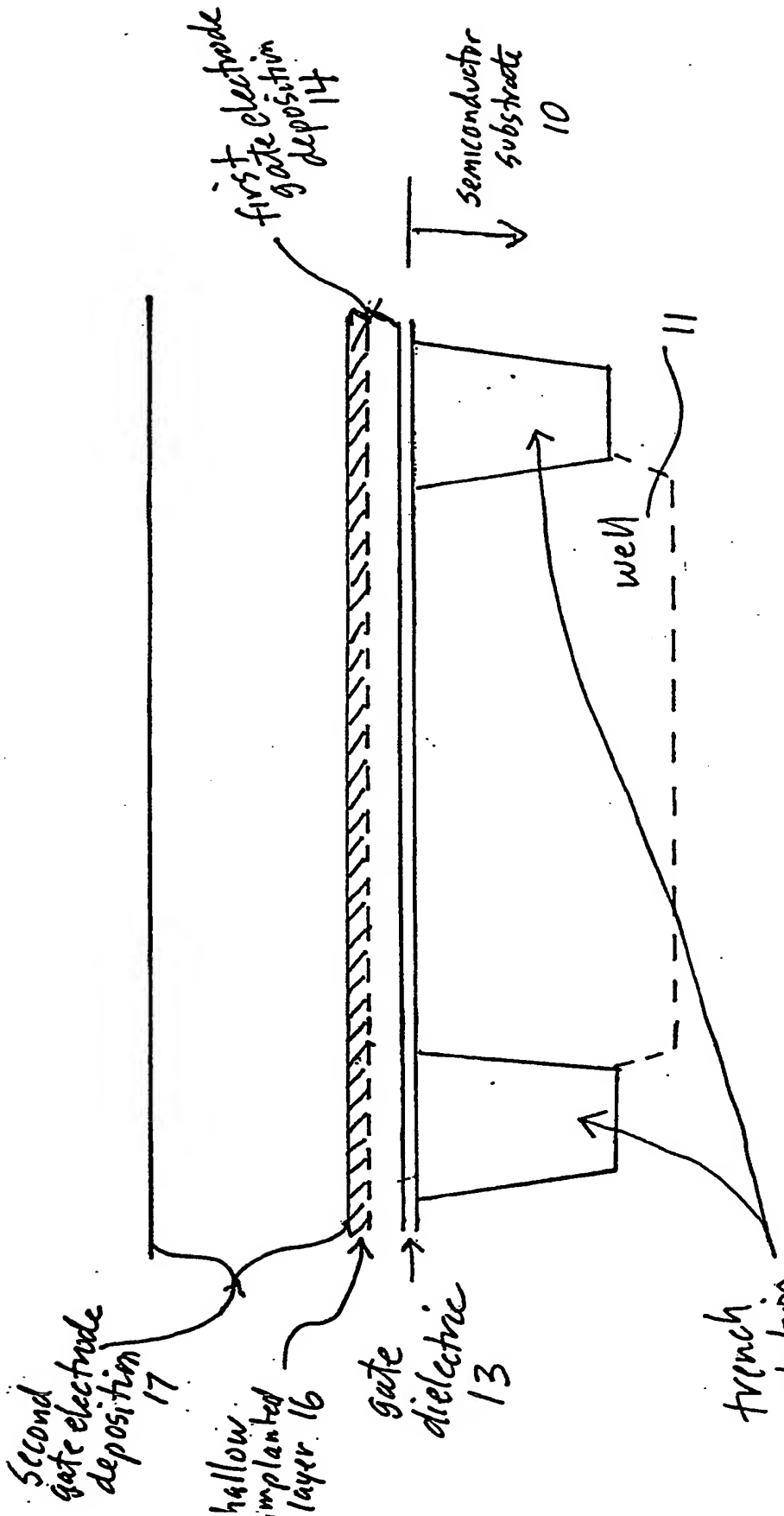

Fig 1c Process through second gate electrode deposition.

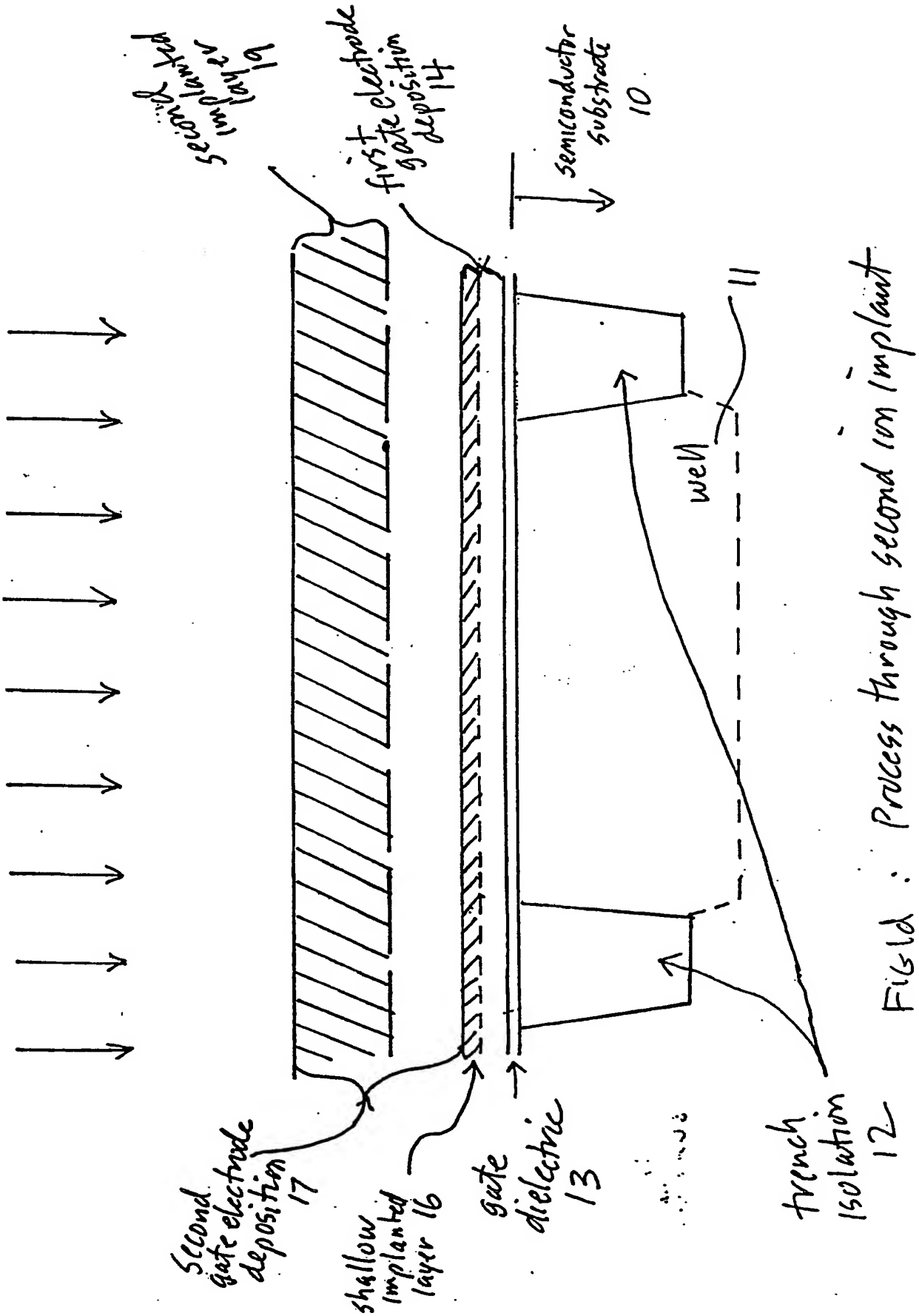

Fig 1d : Process through second ion implant

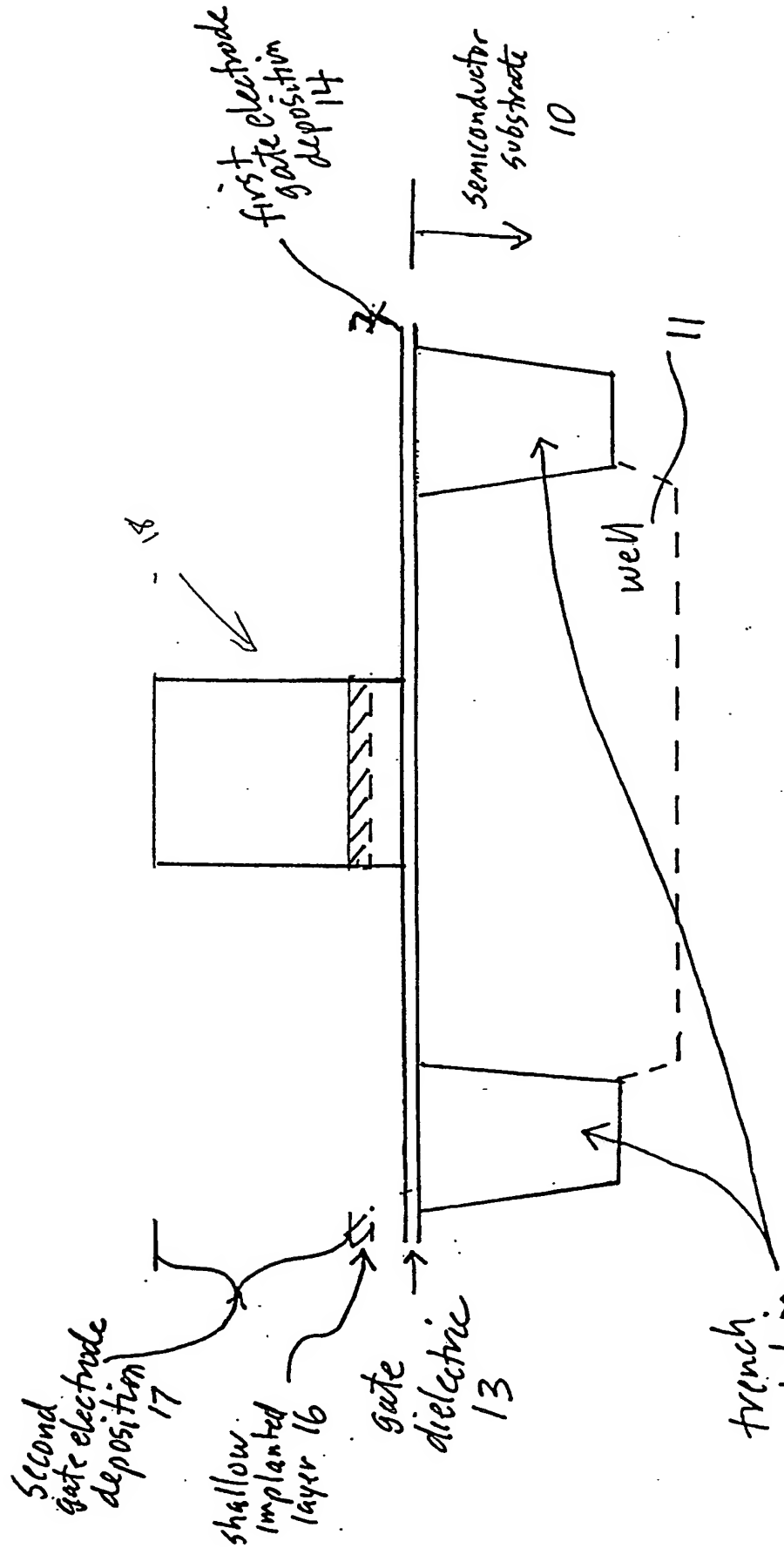

Fig 2g : Process through gate patterning

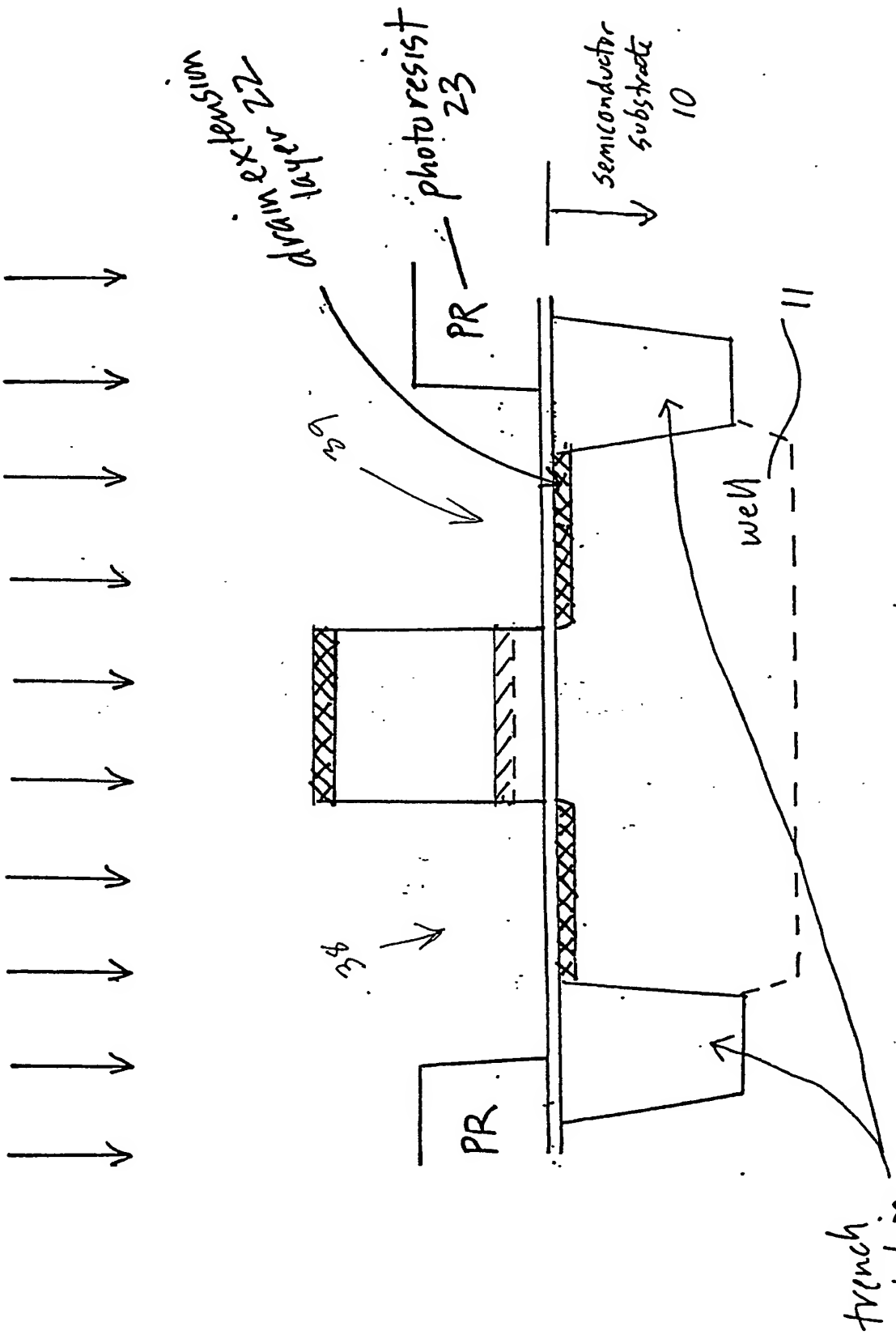

Fig 2b : Process showing Drain Extension implant.

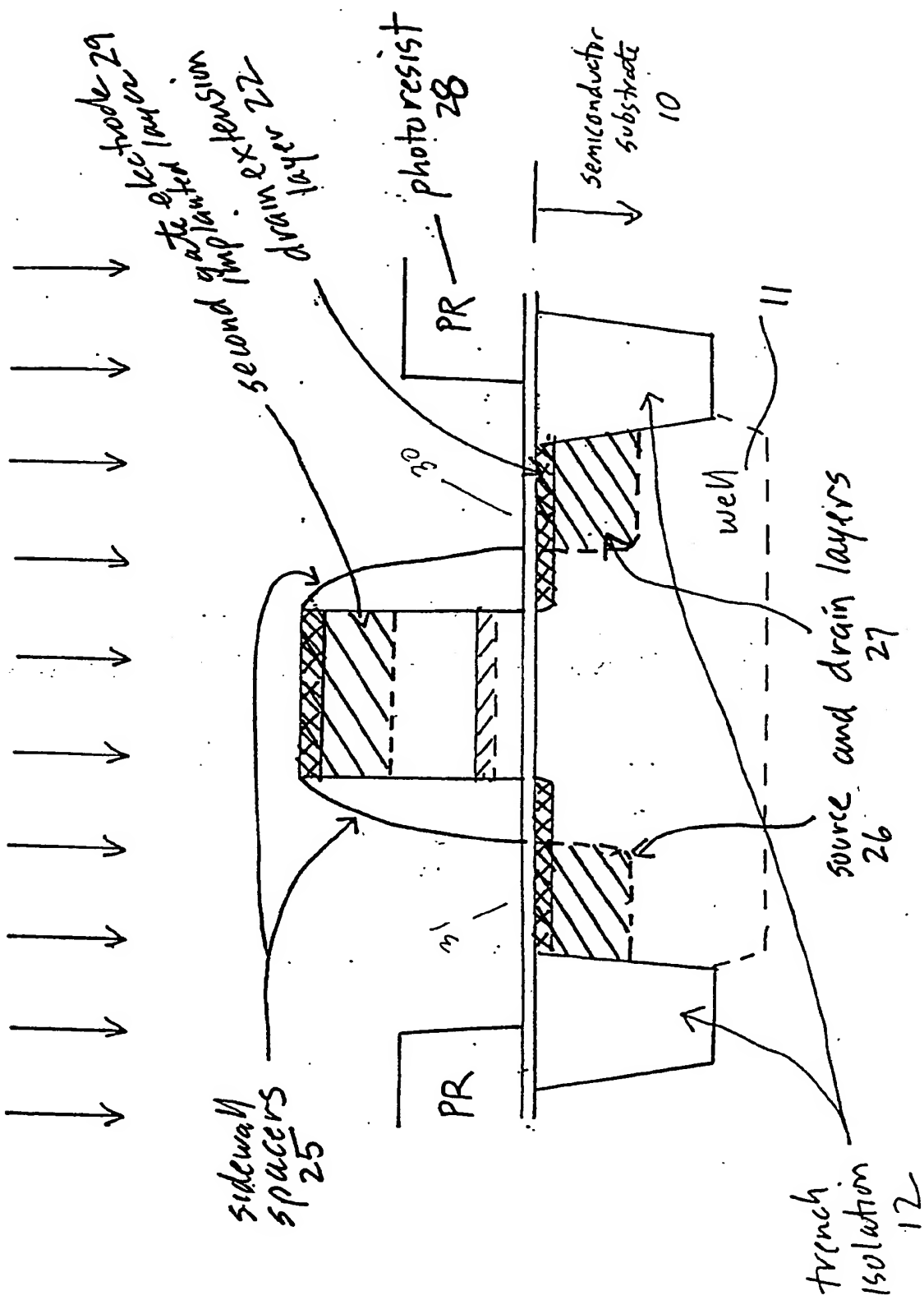

Fig 2c Process showing source and Drain implant providing gate electrode second implant doping.

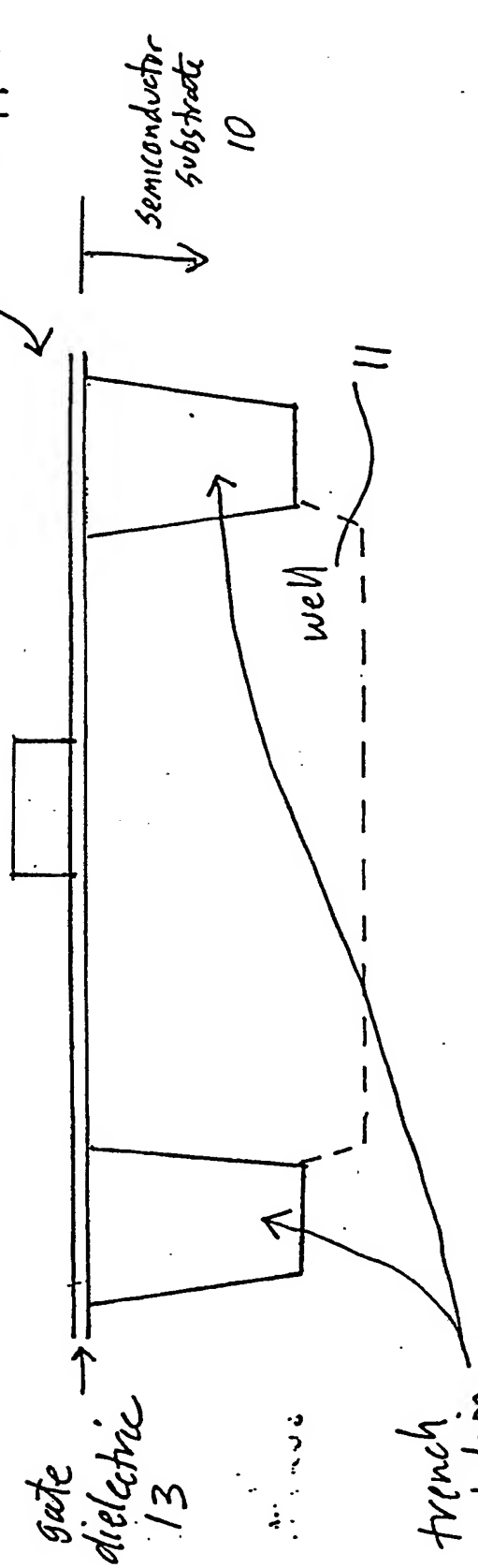

Fig 3g Process through patterning of the first gate electrode

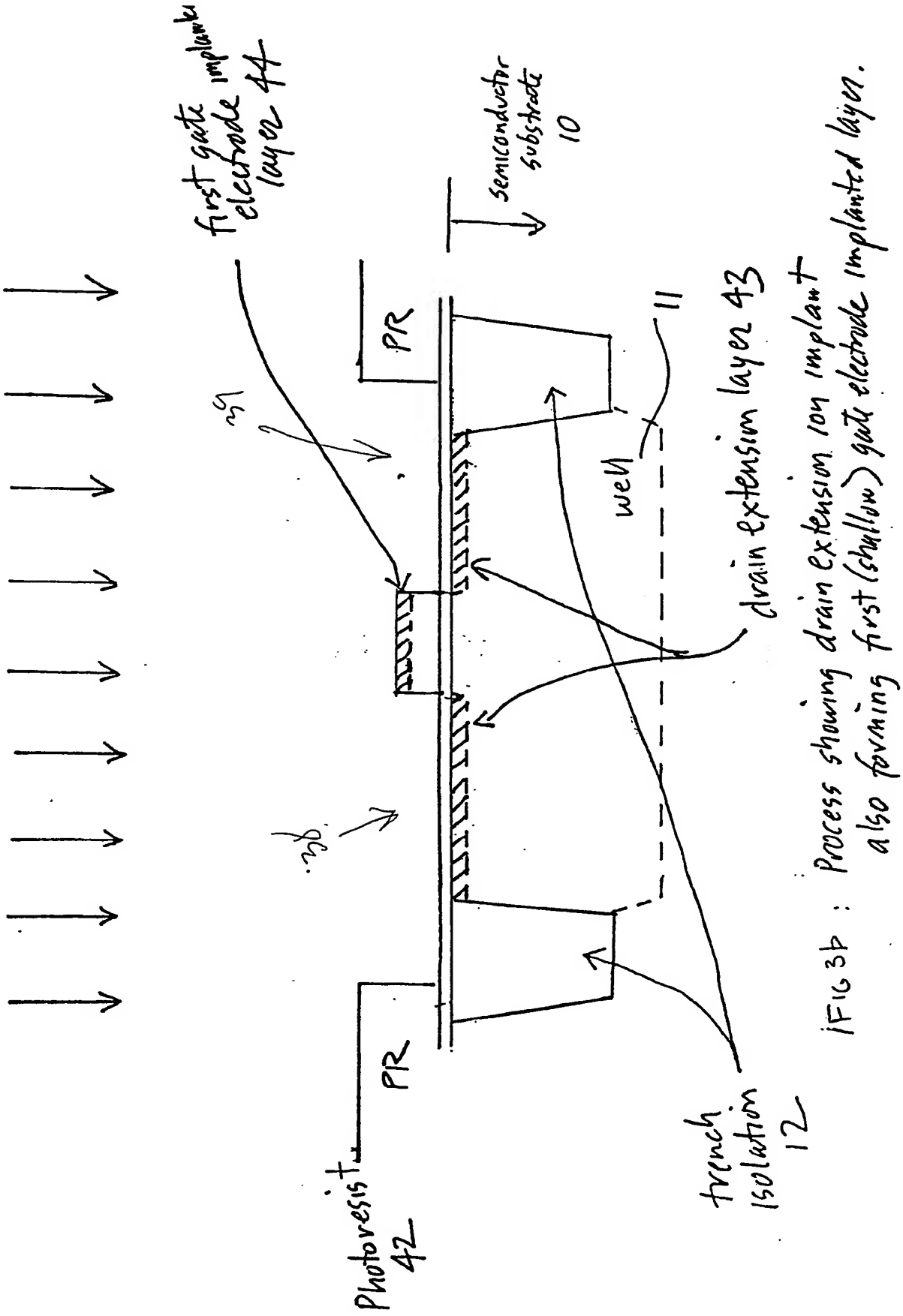

FIG 3b : Process showing drain extension ion implant also forming first (shallow) gate electrode implanted layer.

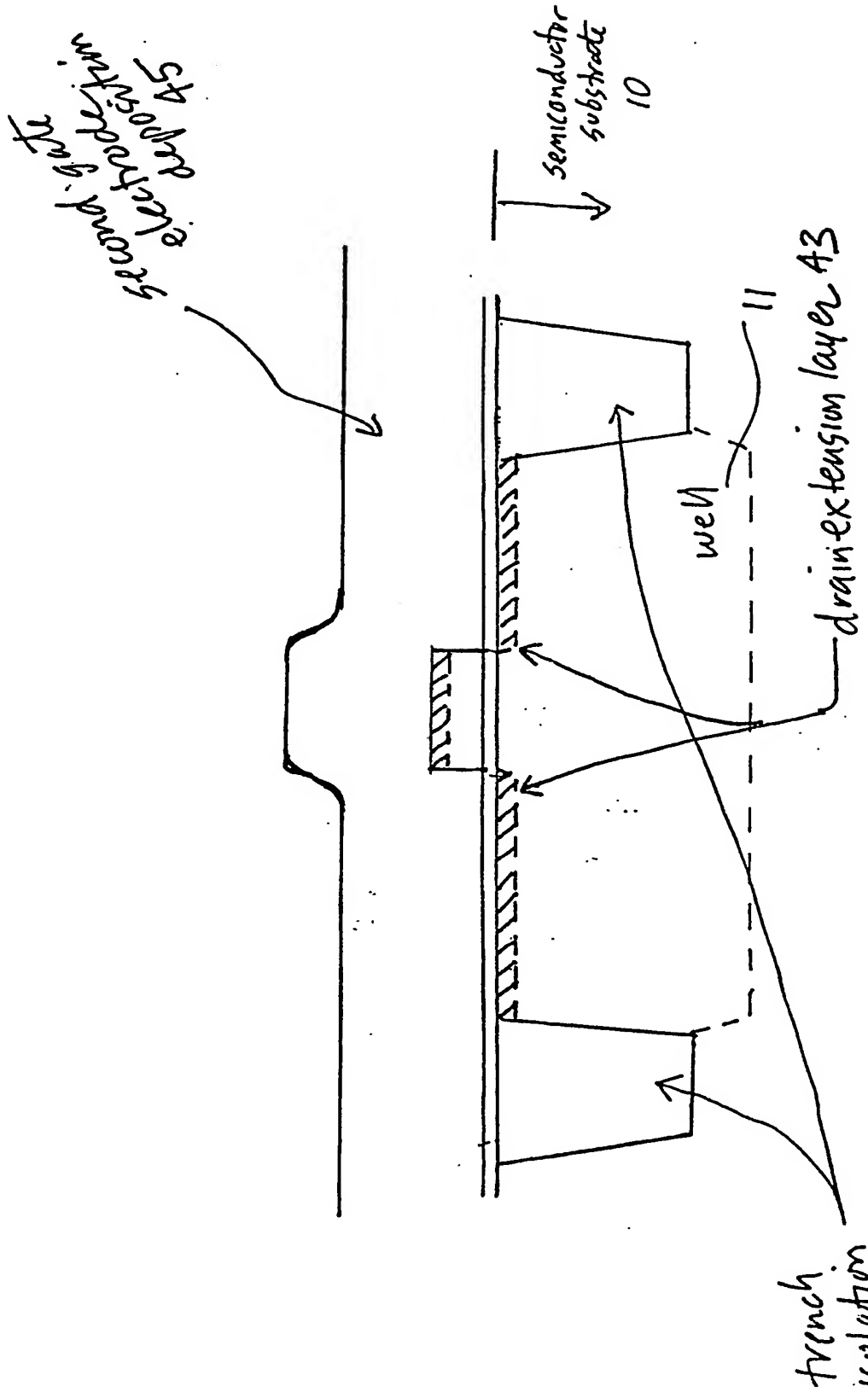

FIG 3C : second Gate electrode deposition

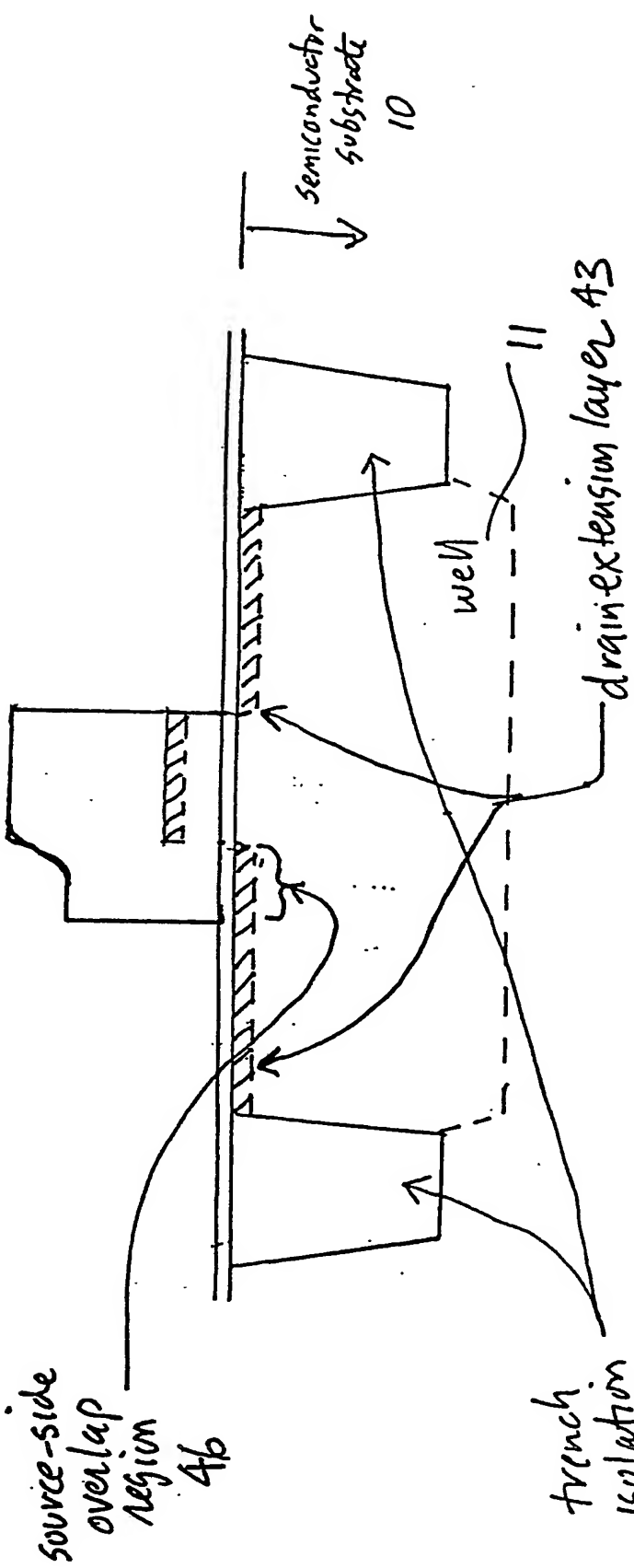

FIG 3A Process showing gate electrode patterning results.

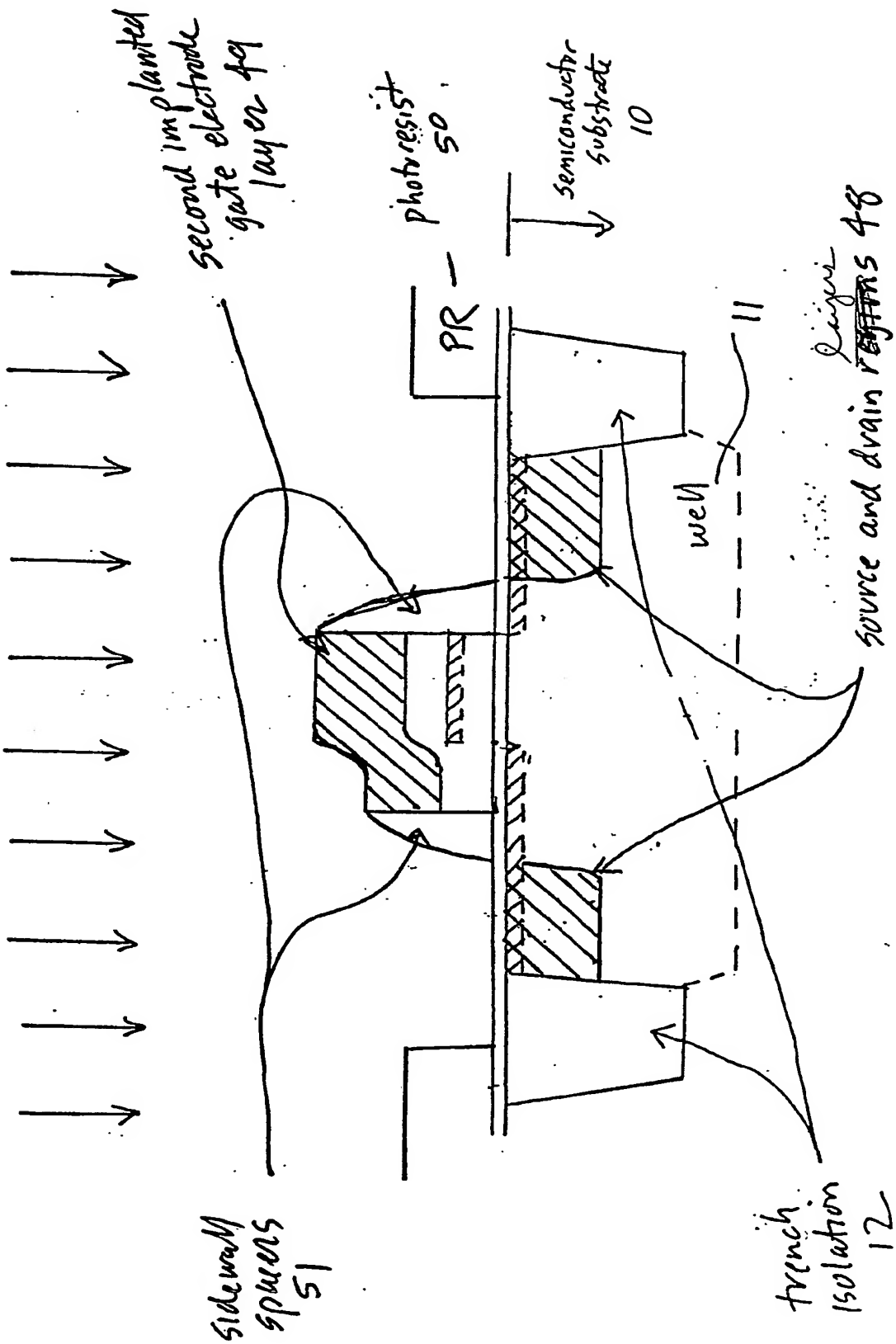

Fig 3e Second Ion implant forms source and drain and second gate electrode implanted layer.

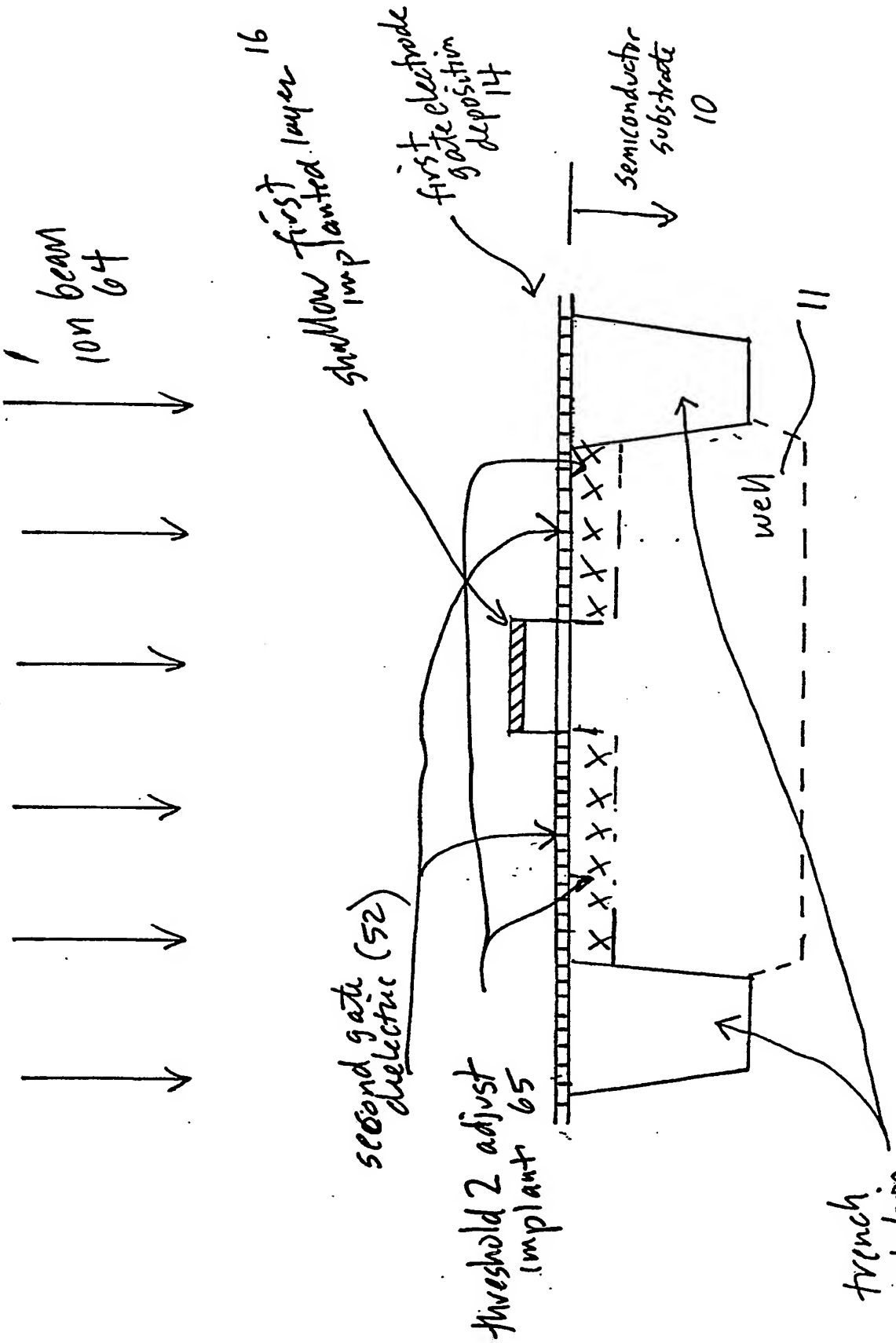

Fig 4a : Processing of the second gate dielectric layer.

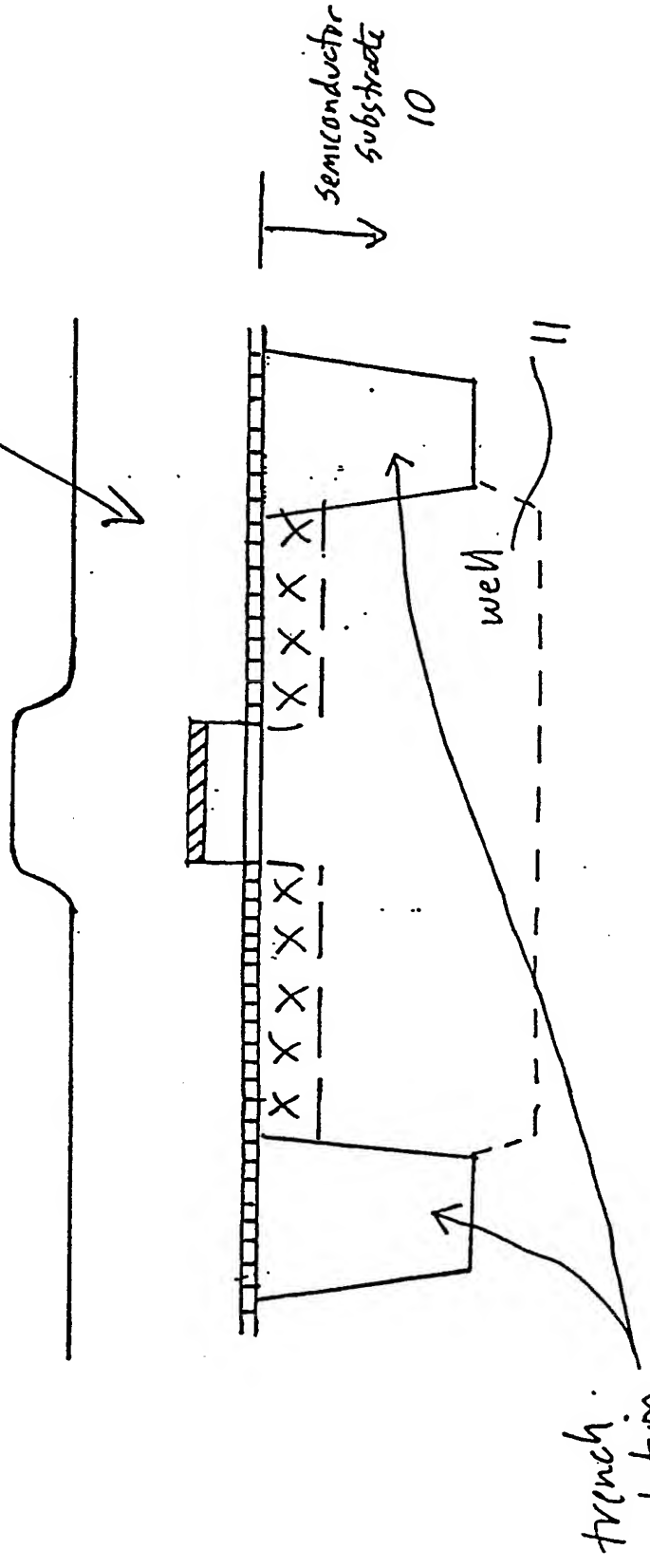

FIG 4B Deposition of second gate electrode layer.

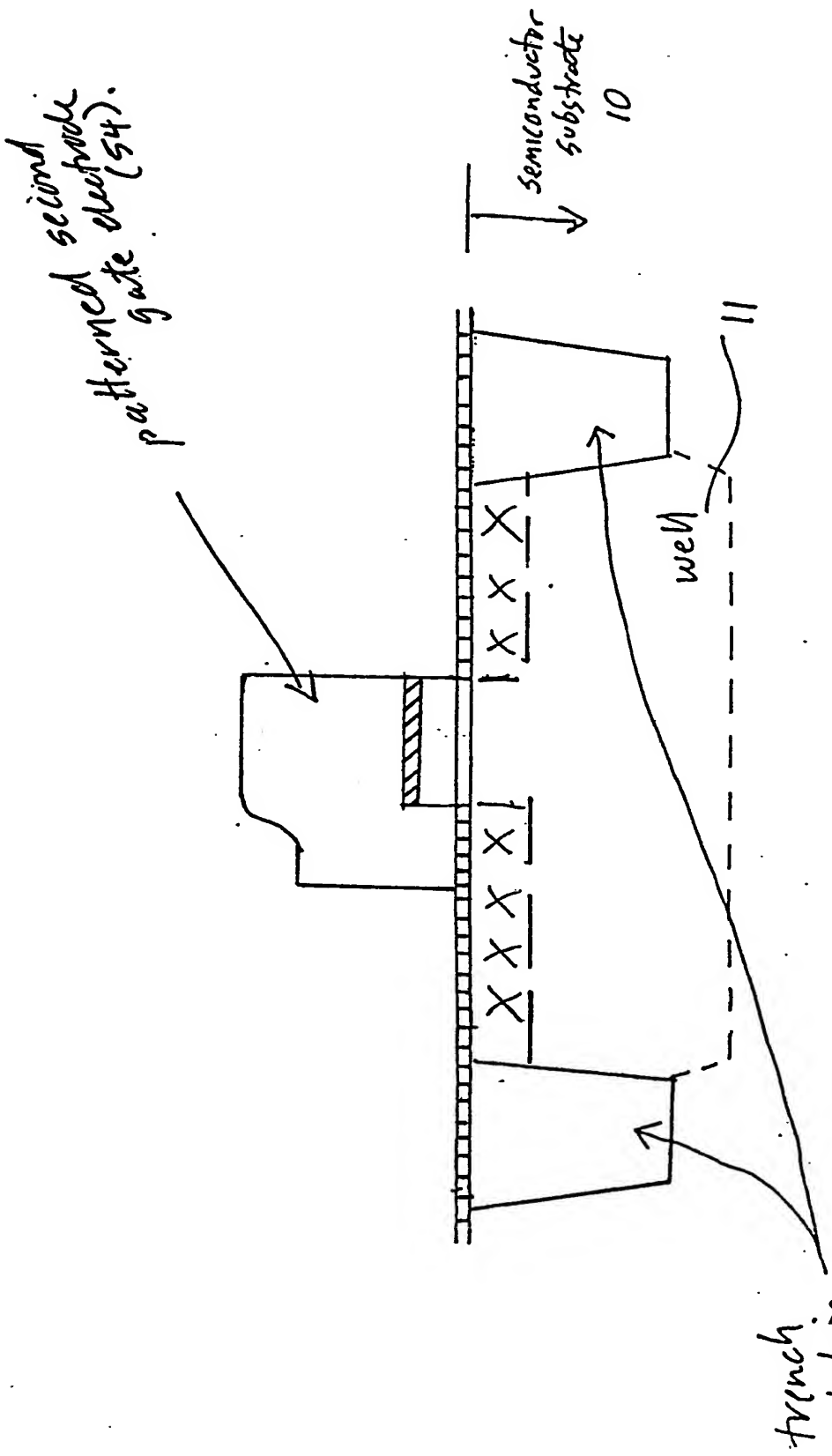

Fig 4c Patterning of second gate electrode.

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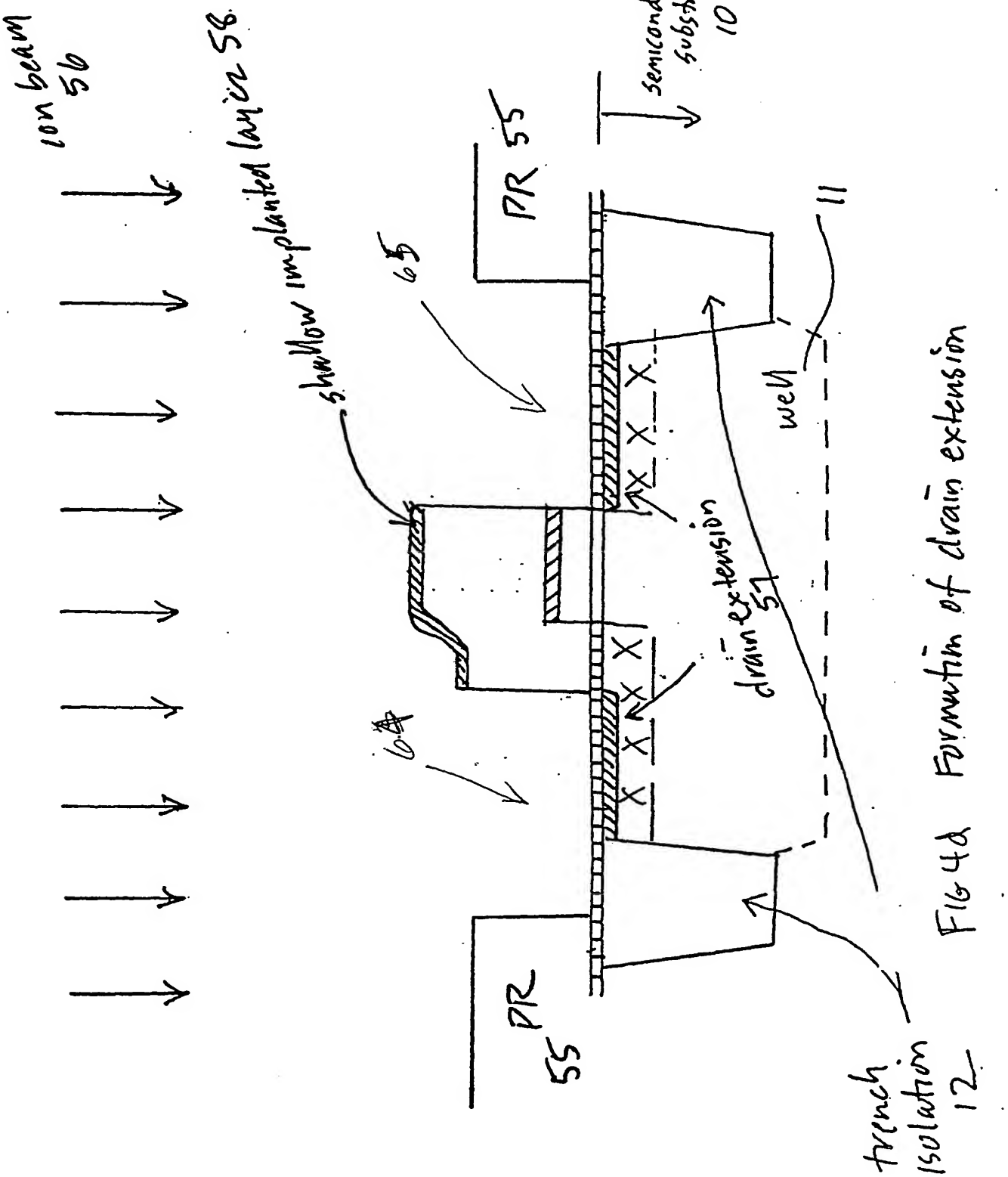

Fig 4d Formation of drain extension

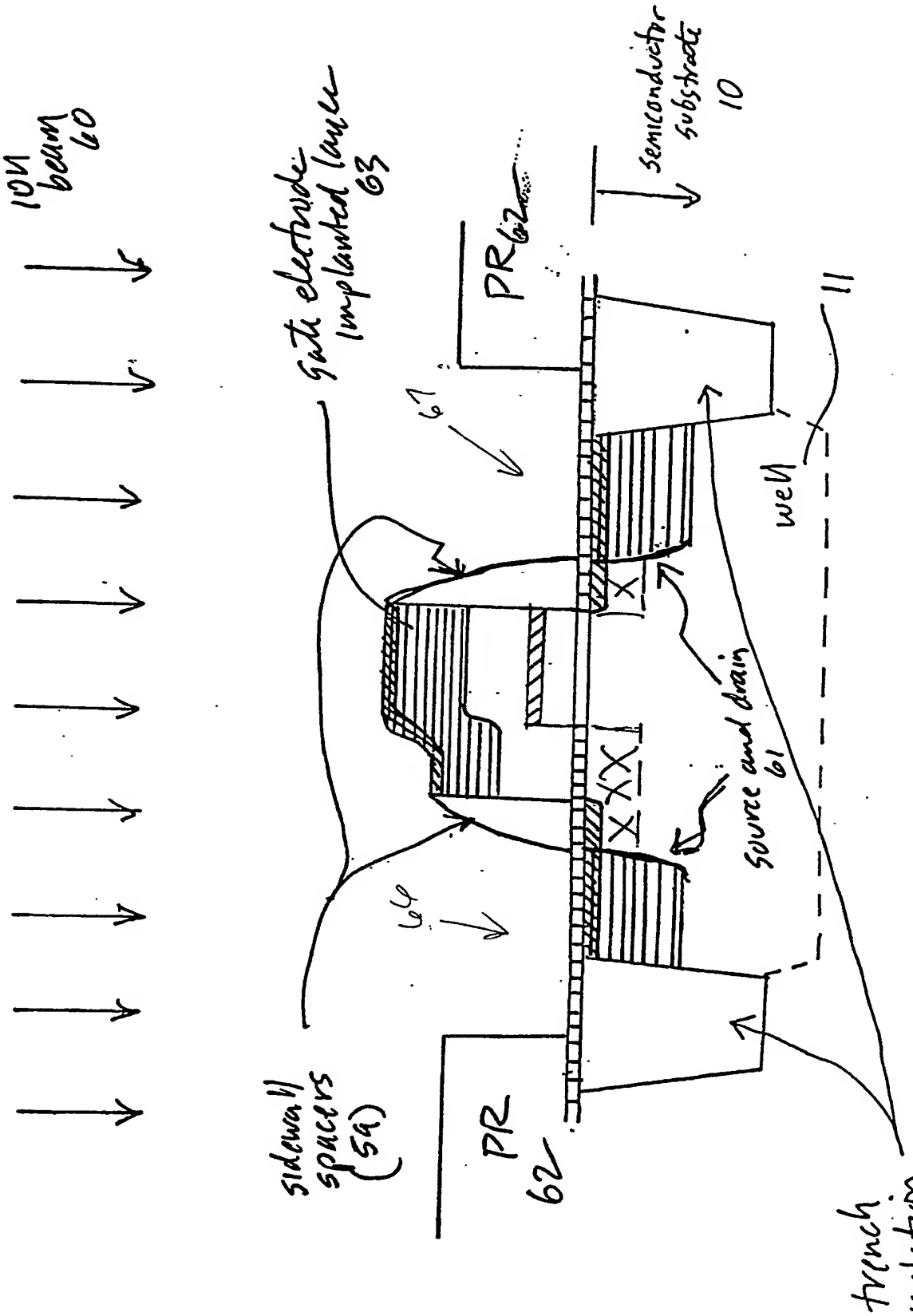

Fig 4e Formation of source and drain

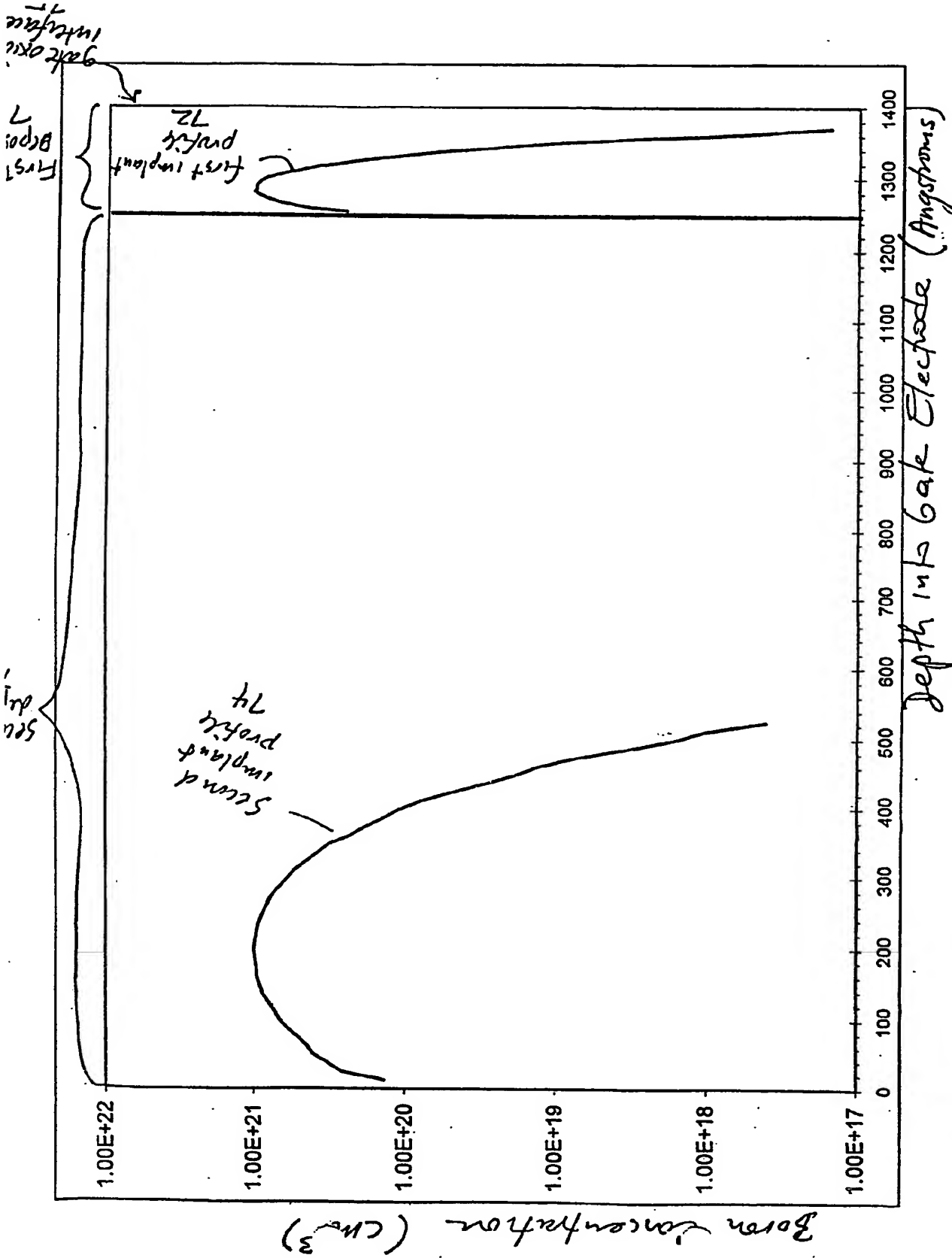

FIG 5 simulation of implant profiles

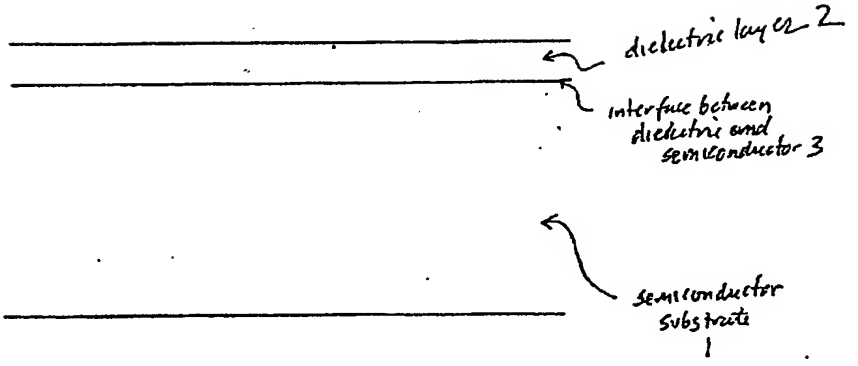

FIG 6 semiconductor substrate with dielectric layer on surface

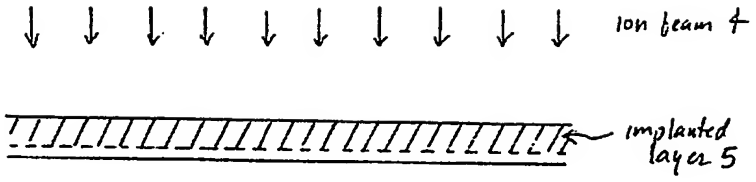

FIG. 7

: ion implant places dopant plus second species into implanted layer contained within dielectric

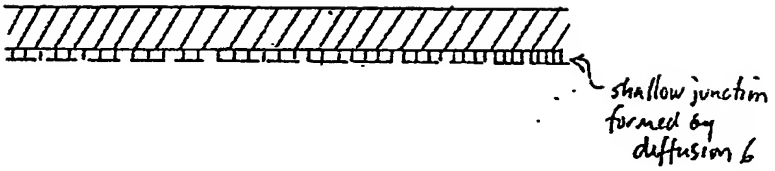

FIG8: After heat treatment, a shallow junction has been formed in the semiconductor substrate.